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**REMARKS**

This application has been revised and the following remarks have been submitted in consideration of the Office Action mailed May 5, 2005. Claims 1-11, 13-27, 29-45, 47-97 remain pending for examination. Claims 1, 15, 33, 52, 66, and 83 are the only independent claims. Claims 12, 28, and 46 have been cancelled without prejudice. Claims 52-97 are new. The claim amendments are fully supported by the specification as originally filed. Specifically, claims 1, 15, 33, and 52-97 are supported by Figures 1-2, corresponding description at paragraphs [0020]-[0028], and the claims as originally filed. No new matter has been added.

Rejection of Claims 1-6, 11, 13-18, 27, 29-32, and 50-51 under 35 U.S.C. § 102(b)/103 in view of U.S. Patent No. 6,356,529 to Hussein

Claims 1-6, 11, 13-18, 27, 29-32, and 50-51 stand rejected pursuant to 35 U.S.C. § 102(b) as anticipated by or pursuant to 35 U.S.C. § 103(a) as unpatentable in view of U.S. Patent No. 6,365,529 to Hussein et al ("Hussein"). Applicants respectfully traverse this rejection in consideration of the amendments made to claims 1 and 15.

Claim 1 is directed to a method for forming an etched pattern on a semiconductor substrate. The method comprises the steps of: depositing a thin film on the substrate; depositing a layer of planarizing material on the thin film; depositing a layer of barrier material that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material on the layer of planarizing material; depositing a layer of anti-reflective coating on the layer of barrier material; depositing at least one layer of

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imaging material on the layer of barrier material; forming at least one first pattern shape in the layers of imaging material, barrier material, anti-reflective coating and planarizing material; removing the imaging material, either after or concurrently with forming the first pattern shape in the planarizing material; removing the anti-reflective coating, either after or concurrently with forming the first pattern shape in the planarizing material; and transferring the first pattern shape to the thin film. Thus, it is a feature of the claimed invention that a barrier layer that substantially prevents diffusion from an interlevel dielectric layer into an imaging is deposited on the layer of planarizing material, it is a further feature that a layer of anti-reflective coating is deposited on said barrier material, and it is a further feature of the claimed invention that at least one layer of imaging material is deposited on the layer of barrier material. Applicants respectfully submit that these features (at least) are neither disclosed nor suggested by Hussein.

Claim 15 is directed to a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor. The method comprises the steps of depositing a dielectric material on the substrate; forming at least one via in said dielectric material, such that at least one of the vias is positioned over the patterned conductor; depositing a layer of planarizing material on the dielectric material and in the via; depositing a layer of barrier material that substantially blocks impurity diffusion from the dielectric material into an imaging material on the layer of planarizing material; depositing a layer of anti-reflective coating on said barrier material; depositing at least one layer of imaging material on the layer of barrier material; forming at least one trench in the layers of imaging material, anti-reflective coating, barrier material and planarizing material, such that at least one of the trenches is positioned over

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the via; removing the imaging material, either after or concurrently with forming the trench in the planarizing material; removing the anti-reflective coating, either after or concurrently with forming the trench in the planarizing material; and transferring the at least one trench to the dielectric material, such that at least one of the trenches is positioned over the via. Similar to claim 1, it is a feature of the claimed invention that the barrier layer prevent substantial diffusion of impurities from an underlying interlevel dielectric layer into an imaging layer. Further, it is a feature of the claimed invention, that a layer of anti-reflective coating is deposited on such barrier layer. Applicants respectfully submit that these features (at least) are neither disclosed nor suggested by Hussein.

Hussein is directed to a method for forming an integrated circuit. In the Office Action, it is correctly noted that Hussein does not expressly disclose the steps of depositing a layer of anti-reflective coating on the barrier material. In the Office Action, it is incorrectly noted that Hussein discloses that the barrier material comprises a material selected from the group comprising silicon or tantalum nitride.

Hussein also fails to disclose these features of the claimed invention. The Hussein ARC layer 108 shown in Figure 3c does not suggest the barrier material of the claimed invention for the following reason. The purpose of the ARC layer 108 is to "reduce reflection at the wavelength of light used in subsequent the photolithographic process." (Hussein, col. 10, lines 61-64). By contrast, the purpose of the barrier material of the claimed invention is to prevent substantial impurity diffusion from the underlying dielectric into the imaging layer. Such is important to prevent resist poisoning. Hussein

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fails to recognize the importance of such barrier material, therefore fails to suggest this feature of the claimed invention.

If Hussein were to be modified to disclose the anti-reflective coating of the claimed invention, Hussein would still fail to disclose the claimed invention for the following reasons. If Hussein were to be modified, Hussein would have two ARC layers 108. Hussein does not suggest the use of two ARC layers 108. Hussein does not teach that use of one ARC layer 108 deficiently reduces the reflection of light, thereby requiring a second ARC layer 108. In fact, Hussein states that “such a material will reduce (or perhaps eliminate) any adverse impact on CD control ...” (Hussein, col. 10, lines 61 – col. 11, line 4). Hussein fails to recognize the importance of the claimed combination of a barrier material, which prevents diffusion, and anti-reflective coating, which reduces reflection, and therefore fails to suggest features of the claimed invention.

Claim 52 is directed to a method for forming an etched pattern on a semiconductor substrate. The method comprises the steps of depositing a thin film on the substrate; depositing a layer of planarizing material on the thin film; depositing a barrier material of silicon dioxide on the layer of planarizing material; depositing a layer of anti-reflective coating on the silicon dioxide; depositing at least one layer of imaging material on the layer of silicon dioxide; forming at least one first pattern shape in the layers of imaging material, silicon dioxide and planarizing material; removing the imaging material, either after or concurrently with forming the first pattern shape in the planarizing material; and transferring the first pattern shape to the thin film. It is a feature of the claimed invention that planarizing material is deposited on the thin film, that a layer of silicon dioxide is deposited on the planarizing material, and at least one

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layer of imaging material is deposited on the silicon dioxide. Applicants respectfully submit that these features (at least) are neither disclosed nor suggested by Hussein.

Claim 66 is directed to a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor. The method comprises the steps of: depositing a dielectric material on the substrate; forming at least one via in said dielectric material, such that at least one of the vias is positioned over the patterned conductor; depositing a layer of planarizing material on the dielectric material and in the via; depositing a barrier material of silicon dioxide on the layer of planarizing material; depositing at least one layer of imaging material on the silicon dioxide; forming at least one trench in the layers of imaging material, silicon dioxide and planarizing material, such that at least one of the trenches is positioned over the via; removing the imaging material, either after or concurrently with forming the trench in the planarizing material; and transferring the at least one trench to the dielectric material, such that at least one of the trenches is positioned over the via. Thus, it is a feature of the claimed invention that a layer of planarizing material is deposited on the dielectric material and in the via. It is a further feature of the claimed invention that a layer of silicon dioxide is deposited on the layer of planarizing material. It is an even further feature of the claimed invention that at least one layer of imaging material on the layer of silicon dioxide. Applicants respectfully submit that these features (at least) are neither disclosed nor suggested by Hussein, as follows.

As previously mentioned, Hussein is directed to a method for forming an integrated circuit. In the Office Action, it is correctly noted that Hussein does not disclose that the barrier material comprises silicon dioxide.

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Hussein also fails to teach these features of the claimed invention. The ARC layer 108 of Hussein fails to disclose silicon dioxide for the following reason. The reason Hussein fails to disclose silicon dioxide as a material for the ARC layer 108 because silicon dioxide is known not to be an anti-reflective layer. As previously mentioned, the purpose of the ARC layer 108 is to reduce reflection in the photolithographic process. If the ARC layer 108 of Hussein were replaced with the silicon dioxide of the claimed invention, Hussein would be rendered unsatisfactory for Hussein's intended purpose. If the ARC layer 108 of Hussein were replaced with the silicon dioxide of the claimed invention, Hussein would no longer reduce reflection in the photolithographic process. For at least this further reason, the claimed invention is patentable over Hussein.

Hussein neither teaches nor discloses a barrier layer deposited on a planarizing material that prevents substantial diffusion from an underlying interlevel dielectric into an imaging material. Further, Hussein fails to disclose or suggest an anti-reflective coating layer depositing on such a barrier layer. Finally, Hussein fails to disclose or suggest use of silicon dioxide as a barrier material. Therefore, Hussein fails to teach the claimed features of the invention.

Accordingly, Applicants respectfully submit that 1-6, 11, 13-18, 27, 29-32, and 50-51 are not anticipated and are patentable in view of Hussein, and therefore request withdrawal of this rejection.

Rejection of Claims 12, 28, 33-36, and 45-49 under 35 U.S.C. § 103(a) as unpatentable over Hussein

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Claims 12, 28, 33-36, and 45-49 stand rejected pursuant to 35 U.S.C. § 103(a) as being unpatentable over Hussein. Applicants respectfully traverse this rejection.

Claim 33 is directed to a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor. The method comprises the steps of: depositing a dielectric material on the substrate; forming at least one trench in the dielectric material, such that at least one of the trenches is positioned over the patterned conductor; depositing a layer of planarizing material on the dielectric material and in the trench; depositing a layer of barrier material that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material on the layer of planarizing material; depositing a layer of anti-reflective coating on said barrier material; depositing at least one layer of imaging material on the layer of barrier material; forming at least one via in the layers of imaging material, barrier material and planarizing material, such that at least one of the vias is positioned over the trench and the patterned conductor; removing the imaging material, either after or concurrently with forming the via in the planarizing material; and transferring the at least one via to the dielectric material, such that at least one of the vias is positioned over the trench and the patterned conductor; removing the barrier material, either after or concurrently with transferring the at least one via to the dielectric material; removing the anti-reflective coating, either after or concurrently with forming the via in the planarizing material; and, removing the planarizing material. It is a feature of the claimed invention that a layer of barrier material that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material is deposited on the layer of planarizing material. It is a further feature of the claimed invention that a layer of anti-

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reflective coating is deposited on the barrier material. It is also a feature of the claimed invention that at least one layer of imaging material is deposited on the layer of barrier material. Applicants respectfully submit that these features (at least) are neither disclosed nor suggested by Hussein.

Hussein is directed to a method of forming an integrated circuit. In the Office Action, it is correctly noted that Hussein does not disclose depositing a barrier material on the planarizing material. In the Office Action, it is incorrectly noted, however, that Hussein discloses a material selected from the group consisting of silicon and tantalum nitride.

Hussein also fails to suggest these features of the present invention. The ARC layer 108 is not deposited on a barrier material. In contrast, the claimed invention requires not only a barrier material, but also an anti-reflective material deposited on such barrier material. All barrier materials are not reflective. For example, it is commonly known that silicon dioxide, while an effective barrier material for preventing diffusion, is not an effective anti-reflective material. The features of both a barrier layer and an anti-reflective layer, therefore ensure both proper diffusion prevention and reflection properties, despite the barrier material chosen. Hussein fails to recognize the importance of both a barrier layer and an anti-reflective layer, and therefore fails to suggest the features of the present invention.

Accordingly, Applicants respectfully submit that Claims 12, 28, 33-36, and 45-49 are patentable over Hussein, and therefore request withdrawal of the rejection.

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Rejection of Claims 7-8, 20-23, and 38-41 under 35 U.S.C. §103(a) as being unpatentable over Hussein in view of U.S. Patent No. 6,391,472 to Lamb III et al.

Claims 7-8, 20-23, and 38-41 stand rejected under 35 U.S.C. §103(a) over Hussein in view of U.S. Patent No. 6,391,472 to Lamb III et al. ("Lamb"). Applicants respectfully traverse this rejection.

Claims 7-8, claims 20-23, and 38-41 each depend ultimately from Claims 1, 15, and 33. It is a feature of these claims that a barrier layer that prevents diffusion is deposited on an planarizing layer, that an anti-reflective layer is deposited on a barrier layer, and that an imaging layer is deposited on the anti-reflective layer. Applicants respectfully submit that these features (at least) are neither disclosed nor suggested by Hussein in view of Lamb, as follows.

As previously discussed, Hussein fails to disclose or even suggest the above-identified features of the present invention. Lamb fails to remedy the deficiencies of the Hussein patent. Lamb does not disclose depositing a layer of barrier material on a layer of planarizing material, depositing a layer of anti-reflective material on the barrier material, and depositing a layer of imaging material on the layer of anti-reflective material. Lamb fails to provide any motivation to modify Hussein in this regard.

Accordingly, Applicants respectfully submit that Claims 7-8, 20-23, and 38-41, which depend from Claims 1, 15, or 33, are patentable over Hussein and Lamb, and therefore request withdrawal of the rejection.

Rejection of Claims 9-10, 19, 24-26, 37, and 42-44 under 35 U.S.C. §103(a) as being unpatentable over Hussein in view of Wolf

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Claims 9-10, 19, 24-26, 37, and 42-44 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hussein in view of Wolf. Applicants respectfully traverse this rejection.

Claims 9-10, 19, 24-26, 37, and 42-44 depend ultimately from Claims 1, 15, 33, and respectively. It is a feature of these claims that a barrier layer that prevents diffusion is deposited on an planarizing layer, that an anti-reflective layer is deposited on a barrier layer, and that an imaging layer is deposited on the anti-reflective layer. Applicants respectfully submit that these features (at least) are neither disclosed nor suggested by Hussein in view of Wolf, as follows.

As discussed previously, Hussein fails to disclose or even suggest the above-identified features of the present invention and Wolf fails to provide any motivation to modify Hussein in this regard. Moreover, with respect to claims 9, 24, and 42 (at least), if Hussein were modified such that the ARC layer 108 comprised silicon dioxide, Hussein would be rendered unsatisfactory for Hussein's intended purpose. As previously noted, it is commonly known that silicon dioxide is not an anti-reflective material. For this further reason, the combination of Hussein and Wolf would not render the claimed invention obvious.

Accordingly, Applicants respectfully submit that Claims 9-10, 19, 24-26, 37, and 42-44 are patentable over Hussein in view of Wolf, and therefore request withdrawal of this rejection.

Rejection of claims 33-36, 42, 45, and 47-49 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,583,047 to Daniels ("Daniels")

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Claims 33-36, 42, 45, and 47-49 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Daniels. Applicants respectfully traverse this rejection.

It is a feature of these claims that a barrier layer that prevents diffusion is deposited on an planarizing layer, that an anti-reflective layer is deposited on a barrier layer, and that an imaging layer is deposited on the anti-reflective layer. Applicants respectfully submit that these features (at least) are neither disclosed nor suggested by Daniels, as follows.

Daniels is directed to a process for forming a microelectronic device. In the Office Action, it is correctly noted that Daniels does not disclose the steps of depositing a layer of barrier material on the layer of planarizing material; depositing at least one layer of imaging material on the layer of barrier material; forming at least one via in the barrier material; and removing the barrier material, either after or concurrently with transferring the at least one via to the dielectric material, either after or concurrently with transferring the at least one via to the dielectric material.

Daniels also fails to suggest these features of the present invention. The Daniels barrier layer shown in Figure 6d. is not deposited on the planarizing material, but instead the low-k dielectric. In other words, while Daniels sandwiches the barrier layer between the photoresist and dielectrics, the claimed invention sandwiches the barrier layer between the anti-reflective layer and the planarizing material. In addition to this feature of the claimed invention, Daniels fails to disclose an anti-reflective layer on the barrier layer. For at least these reasons, the claimed invention is patentable over Daniels.

Accordingly, Applicants respectfully submit that Claims 33-36, 42, 45, and 47-49 are patentable over Daniels, and therefore request withdrawal of this rejection.

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Rejection of claims 38-41 under 35 U.S.C. § 103(a) as unpatentable over Daniels in view of Lamb

Claims 38-41 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Daniels in view of Lamb. Applicants respectfully traverse this rejection.

Claims 38-41 depend from claim 33. It is a feature of the Claim 33 that a layer of barrier material that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material is deposited on the layer of planarizing material. It is a further feature of Claim 33 that a layer of anti-reflective coating is deposited on the barrier material. It is also a feature of the Claim 33 that at least one layer of imaging material is deposited on the layer of barrier material. Applicants respectfully submit that these features (at least) are neither disclosed nor suggested by Daniels in view of Lamb, as follows.

As discussed previously, Daniels fails to disclose or even suggest the above-identified features of the present invention and Lamb fails to provide any motivation to modify Hussein in this regard. Daniels does not disclose a barrier material that prevents diffusion from an underlying interlevel dielectric into an imaging material that is deposited on planarizing material. Further, Daniels does not disclose an anti-reflective layer that is deposited on the barrier layer. Lamb does not provide any motivation to modify Daniels in these regards. For these reasons, the claimed invention is patentable over Daniels in view of Lamb.

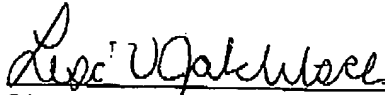
Accordingly, Applicants respectfully submit that Claims 38-41 are patentable over Daniels in view of Lamb, and therefore request withdrawal of this rejection.

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Respectfully Submitted,

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